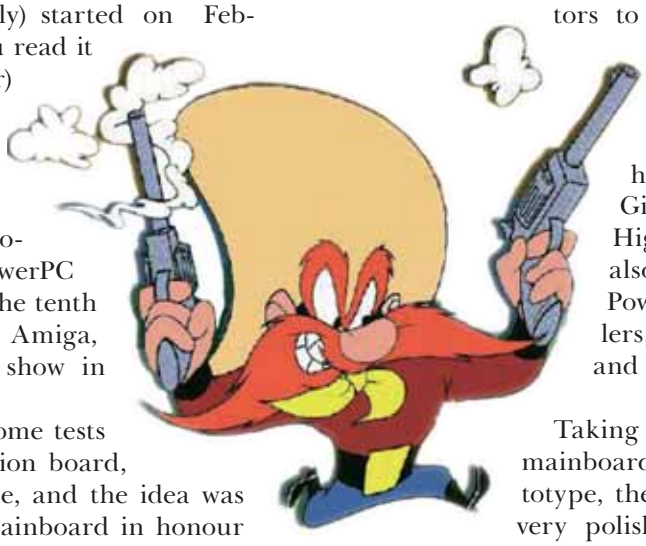
CODENAME: SAMANTHA

THE MISTERY UNCOVERED, FINALLY!

By Stefano Guidetti and Nicola Morocutti

Translation by Stefano Guidetti and Varthall

Sam, Sam and again Sam! In the last few months we heard very often about this "Sam". But what Sam really is? Is it a nickname for Samantha? Does it stands for Simple Amiga Motherboard? A rocket launcher? A character from a japanese cartoon ("Koya no shoonen Isamu" perhaps)? No, none of this.
SAM is simply the codename of a project (completely made in Italy) started on February 2006 (yes, you read it correctly, THIS year) and that has found its fullfillment this September with the official presentation of the first prototypes of a new PowerPC mainboard during the tenth edition of Pianeta Amiga, the biggest Amiga show in Italy.
It all started with some tests on a 440EP evaluation board, codenamed Yosemite, and the idea was to name the new mainboard in honour of the famous cartoon character Yosemite Sam, and so it was: SAM was born!



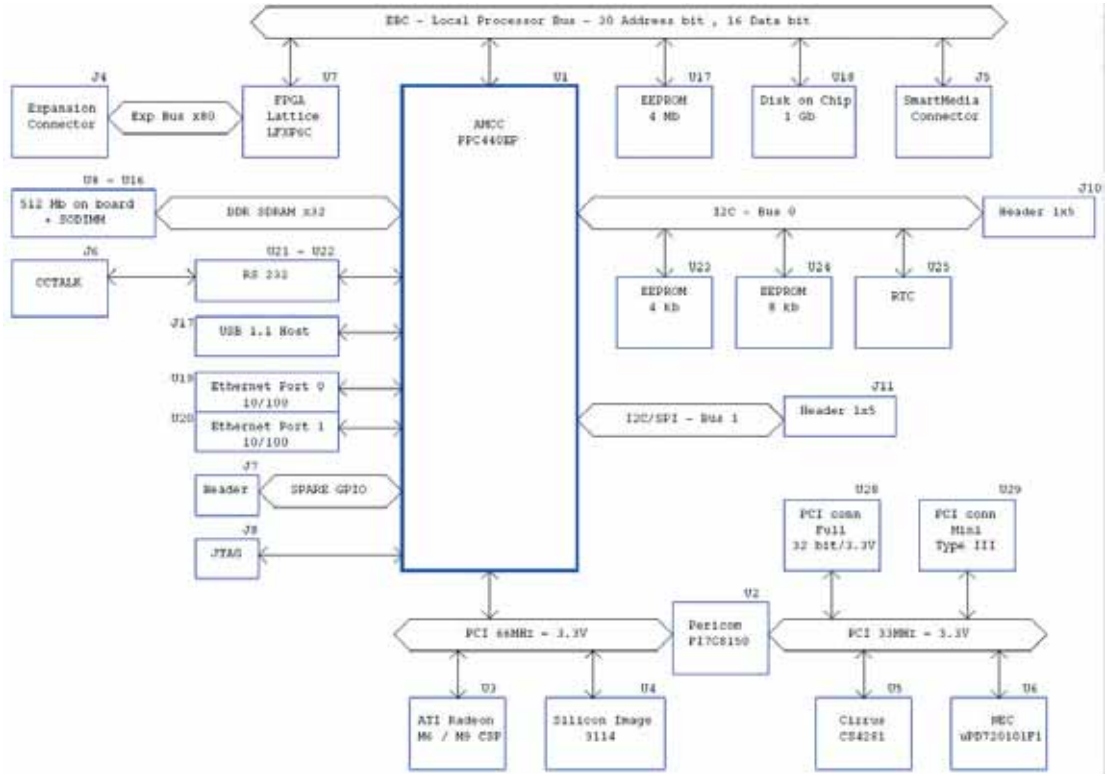
A look under the hood

Sporting a dimension of 17x17 cm the new board has a Mini-ITX form-factor. Its highlights are a very small footprint (the board height is about 2cm) and a high density of components mounted on both sides, using all the available space to mount the highest number of devices and interfaces and to be able to offer a high grade of versatility, expandibility and customization.

Although the form factor is the same as the MicroA1, SAM has much more modern specs: RAM DDR 266, more powerful onboard graphic chip, Serial ATA controller, USB 2.0 and, if that's not enough, it features a very interesting onboard FPGA connector, opening the possibility to expand the board by adding new functionalities.
Just to make an example: it's possible to use the FPGA to emulate, in hardware, the Amiga chipset, like it's done on the Minimig. It would be sufficient to build a card with a 68000 compatible processor, some memory and keyboard, mouse and monitor connectors to get full compatibility with older software.
But that's only the beginning... it's possible to implement in hardware something like GigaEthernet controllers, High Speed UART and also CPUs (i.e. another PowerPC!), microcontrollers, AD & DA converters and much more...

Taking a closer look at the mainboard (although only a prototype, the printed circuit seems very polished with golden contacts) we can see that the board is composed by the following parts:

- Power unit for a standard ATX PSU. The board can have a vertical or horizontal connector to fit to very small cases.
- Memory: on the 512MB version we find 4 DDR 266 banks on the upper side and 4 banks on the bottom side of the board. Optionally a DIMM 100 pins slot can be installed for another memory expansion of 512MB, for a total 1GB of addressable



memory.
- Video: an onboard ATI Radeon Mobility M9, with 64MB of graphic memory directly integrated on chip.
- CPU: placed on the center of the board, we will talk more about that later.
- PCI devices and slots, placed on the left side of the board: audio controller, USB2.0 controller, PCI-PCI bridge, Serial ATA controller, 1 full PCI slot and 1 optional mini-PCI slot (on the bottom side of the board).
- FPGA and Flash memory devices, placed on the bottom center of the board under the CPU: 1 FPGA Lattice XP, 1 EPROM for UBoot, 1 optional socketed DiskOnChip, an FPGA expansion connector and an optional Smart Media Card connector on the bottom side of the board.
- External connectors, placed all in a row to give the board a low profile: Audio OUT, 2x USB, S-Video, DVI, DB9 serial, 2x ethernet.

On the board there's a certain number of connectors, too: 4 Serial ATA connectors, 2 supplemental USB2.0 connectors, another USB1.1 connector, 1 VGA and 1 LVDS connector, CD/DVD in, audio in, audio out, mic in, line in, 2 I2C connectors, 1 34 pins GPIO expansion connector, 1 JTAG connector (used for CPU debugging).

Let's examine more deeply the board: the core of SAM is the PowerPC 440, a System On Chip (SoC) produced by AMCC under licence from IBM. One of the main features of such a chip is the presence, together with the CPU, of a number of integrated peripherals. This makes it possible to build a complete system with a huge saving of (both development and debug) time, components, space used on the PCB and, last but not least, a minor cost for the final user.
As a practical consequence, on the board the classical northbridge/southbridge combo (like the ArticiaS/VIA686B on the micraA1) is missing, as their functionalities are partially integrated on the CPU and, for what is left out, provided by other components and devices.

For the specific model of CPU mounted on SAM, the 440EP, we have the following integrated peripherals:
- DDR memory controller
- PCI controller
- Flash memory devices controller
- USB 1.1 host and USB 2.0 device controller
- 2 Ethernet 10/100 controller
- Up to 4 serial ports

- 2 I2C interfaces
- SPI interface
- 64 pins for General Purpose I/O

Phisically the 440EP is a chip of 35mmx35mm, with a PBGA packaging with 456 pins. It's built with CMOS (0.13 um) technology, has a very low power consumption (only 3 Watt at 533Mhz) and it does not require any active cooling system.

But let's start with the CPU features.

The PowerPC 440EP core features a 7 stage pipeline and is able to execute up to 2 instructions per cycle with a performance of 1334 Dhrystone and 2.1 Mips at 667Mhz. To further increment the performance, the "core" has a dynamic branch prediction unit and 24 DSP instructions.

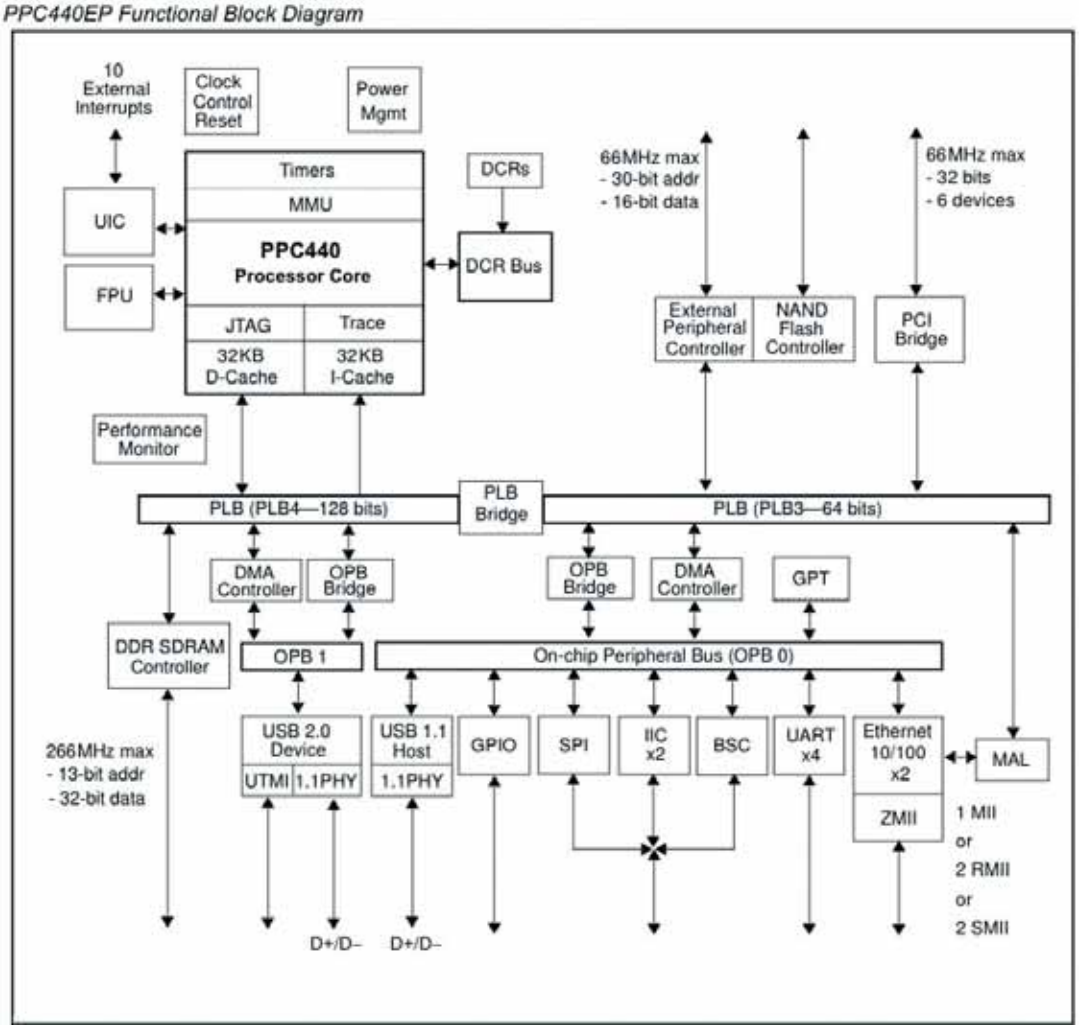
There are two first level caches: both 32k for data and instructions, 64-way set associative, non blocking and supporting both write-through and write-back modes. The 400EP (as the GR version and unlike the GP, GX, SP and SPX ones), includes a high performance FPU, with a 5-way pipelines. This superscalar unit supports both single and double precision operations (IEEE 754) using 32 64-bit registers, and can execute up to one instruction per cycle.

The CPU is interfaced to the controller of the onboard memory by a 128bit PLB4 bus (Processor Local Bus), with separate high performance, read-write busses with a throughput of 4.2GBps.

The memory controller has a 32 bit interface with 13 address bits and supports upto 4 DDR 266 memory banks of 256 MB each, for a maximum of 1 GB; CAS latency can be set to 2, 2.5 or 3 and the throughput is 1.1 GBps.

Linked to the PLB4 with a crossbar is a second 64 bit PLB3, to which are interfaced both the PCI and the EPC (for external peripherals) controller. The 32 bit PCI controller complies to the 2.2 standard, can

PPC440EP Functional Block Diagram



operate at a 66MHz maximum frequency and has an interface providing a 3.3V line.
The CPU may execute code at boot time also from any memory available on the PCI bus.
On the EPC bus there's a NAND flash memory devices controller, supporting upto 4 256MB devices in DMA mode (thus transfering data blocks from the flash to the SDRAM memory with no CPU usage).
On the controller a SmartMedia Card connector can be added.
These devices can be used as mass storage devices, optionally bootable.
Other onboard devices, such as USB, Ethernet and I2C, which don't need a high total throughput, are served through an 30 bit OPB (On-chip Peripheral Bus) running at 83 MHz max.
Both 10/100 Ethernet full duplex ports work in DMA, too.
The USB controller has both a host 1.1 type and a device 2.0 type interface. Only the first is implemented on Sam, since the second one is usually found on printers and other similar external devices.

SAM440EP PCB just after being printed

The board's strongest point is the high level of expandibility thanks to its FPGA. The chip used on this prototype is from the Lattice XP family, with 5.8K LUTs, 188 I/O pins, 72 Kbits of Block Ram, and 23Kbits of Distribuited Ram.

The FPGA is directly connected to the CPU by the EPC bus, running at 66MHz. It can be accessed through a 96 pins connector, on 4 rows with a 2 mm step, offering upto 80 pins for the I/O.

All the documentation regarding this connector's specifications and FPGA usage will be released free of charge.
It's worth noting that, during production phase it's possible to choose a different FPGA from the same family, but with a higher capacity, since all the FPGAs are pin-compatible.
Those who prefer easier to build hardware add-ons can use the GPIO connector (step 2.0 mm) which gives access to 30 generic I/O pins of the CPU (with one of them generating interrupts), like on the good old Amiga 1200 and its clock port.

Let's talk now about the PCI bus. Most of the devices are connected to this bus; for best performance a PCI-PCI bridge from Pericom has been used, which manages the slower and faster devices separately. On the primary 66 MHz bus we can find the ATI Radeon chip and the Silicon Image 3114 Serial ATA controller, while on the slower secondary bus (33 MHz) we find the Cirrus Logic audio chip, the Nec USB 2.0 controller and two PCI and MiniPCI slots.

As previously noted the graphic chip is an ATI Radeon Mobility M9 (a member of the 9000 family), with 64MB DDR RAM on chip and an internal 128 bit bus. The chip's frequency is 250 MHz, while RAM runs at 200 MHz with a RAM DAC of 400 MHz.The maximum resolution for both 2D and 3D is 2048 x 1536. The available video outputs are DVI and S-Video on the back panel, and VGA and LVDS 50 pins on internal header.

Audio is managed by the Cirrus Logic CS4281 chip, having 4 DMA controllers DMA with bus mastering which can handle up to 4 indipendent audio streams (up to 8 channels) and has 2 frequency converters. It's connected to a AC97 codec, a

Cirrus Logic CS4299, with 20 bit DA and 18 bit AD converters.
These are the I/O connectors: 3.5 jack for audio out, an internal CD/DVD connector and a last internal connector on header for audio in, audio out, mic in, PCM in and PCM out, to be preferably connected on the front audio panel available on many modern cases. A MIDI / joystick connector isn't available.

The NEC controller is a multifunction chip, offering 2 USB OHCI controllers (1.5 and 12 Mbps) and an USB EHCI one (full speed 480 Mbps) for a total of 4 USB ports, 2 internal and 2 external. Remember that the CPU has an additional USB 1.1 port.

The PCI connector allows the use of 3.3V cards only. These can be recognised as the key on the PCI connector is in a different position as the one on 5V cards, so the latter can't be mounted in our connector.
Most of the modern cards have both keys, these can be used on both type of slots (3.3V and 5V). The MiniPCI slot, located in the lower part of the motherboard, is a 124 pin type 3 one.

The remaining, still not mentioned interfaces and connectors include:
- a serial 8 pins interface, with a maximum speed of 200000 BPS, DMA supported, NS16750 compatible
- optional serial cctalk interface, for connection to payment devices such as coin acceptors, bill/note acceptors and coin hoppers
- 2 10/100 full duplex ethernet interfaces, SMII, DMA supported
- a PLCC socket for a flash EPROM for UBoot, 512KB sized
- a 32 pins dip socket for DiskOnChip 2000 devices which, by means of a flash memory, can be used as a hard drive from 16MB up to 1 GB, with boot capabilities
- a Real Time Clock on I2C bus, with 512 bytes of RAM
- a coin type battery, 3.0V type CR2032
- 2 EPROMS on I2C bus, one by 512 bytes containing code for CPU bootstrap, and one by 1024 bytes for UBoot variables

For more information on the PPC 440EP CPU and on the 440 family in general visit the AMCC site at ***http://www.amcc.com***, and on the XP FPGA family the Lattice site: ***http://www.latticesemi.com.***

Conclusions

With this technical overview we end the preview of this new PowerPC board which aims to run the highest number of operating systems. AmigaOS4, MorphOS, Linux and Aros, too: everyone is welcome on this board which, at least by the intentions of its developers, doesn't want to limit any use of it. May it be that, after so many years of divisions and resentments, a reunification can finally begin?